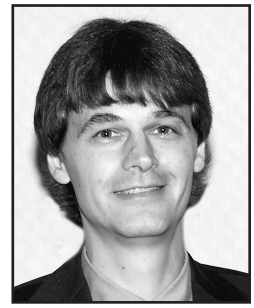
Session 27 Overview

DRAM and eRAM



Chair: Martin Brox, *Qimonda, Neubiberg, Germany*

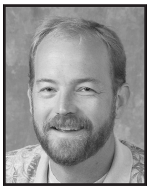
Associate Chair: Kazuhiko Kajigaya, *Elpida Memory, Sagamihara, Japan*

Demand growth for electronic systems has been driven by new consumer and computing applications. The most popular examples are the next-generation, high-resolution game-consoles. These systems heavily leverage the performance of today's memories and processors. Yet, these applications are still unable to create a life-like experience due to the limitations of the on- and off-chip memory bandwidth available to the processing functions. Careful optimization of the memory hierarchy bandwidth is necessary to improve system performance. High-speed embedded-DRAM (eDRAM) has evolved as a serious contender to embedded-SRAM (eSRAM), while external data-rates continue their rapid rise. However, speed improvements cannot stand on their own as system costs must be kept reasonable. To this end, good test and repair solutions reduce cost and facilitate higher levels of integration. The presentations in this session report recent advances that address these challenges.

Paper 27.1 by IBM introduces an innovative sense-amplifier for use in an eDRAM macro operating at a random-cycle frequency of 500MHz. This macro, which occupies only 32% of an equivalent eSRAM-macro in the same SOI-technology, enables higher-density cache implementations improving system level performance.

Cost, test strategy and system integration are the focus of the next two presentations. Paper 27.2 by Renesas, Shikino and Daioh, explores strategies needed for known-good-die (KGD) applications with the example of an eSRAM-macro. KGD is a pre-tested die that guarantees the full-spec operation, which is indispensable for cost-effective multi-chip package (MCP) applications. MCPs are implemented in almost all new cell phones and will be widely implemented in the consumer applications soon. Paper 27.3 by Renesas describes a DDR2-memory-interface for consumer applications. This interface uses an I/O loop-back measurement technique which is fully integrated into the DDR2-clocking system.

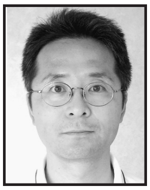
Continuing from last year's ISSCC, graphics devices resume to increase external bandwidth. Paper 27.4 by Samsung establishes the new benchmark by demonstrating a data-rate of 4Gb/s/pin with the recently finalized GDDR4 standard. Implementation details of the high-speed single-ended interface are presented. Paper 27.5 by Micron presents a second GDDR4 device that conquers the battle of deterministic clock-domain management necessary to achieve a data-rate of 2.5Gb/s/pin in a double-data-rate interface. This device implements GDDR3 and GDDR4 operating modes on the same chip, providing flexibility for the consumer market. The last paper of the session by KAIST and Samsung demonstrates a jitter-resistant DLL architecture capable of 1GHz clock-frequency required for a 2Gb/s/pin data-rate and details a solution to reduce DLL jitter in a noisy, on-chip memory environment.



27.1 A 500MHz Random Cycle 1.5ns-Latency SOI Embedded DRAM Macro Featuring a 3T Micro Sense Amplifier 1:30 PM

J. Barth, IBM, Burlington, VT

A prototype SOI embedded DRAM macro is developed for high-performance microprocessors and introduces a performance-enhancing 3T micro sense amplifier architecture (μSA). The macro was characterized via a testchip fabricated in a 65nm SOI deep-trench DRAM process. Measurements confirm 1.5ns random access time with a 1V supply at 85°C and low voltage operation with a 600mV supply.



27.2 A 65nm Embedded SRAM with Wafer-Level Burn-In Mode, Leak-Bit Redundancy and E-Trim Fuse for Known Good Die 2:00 PM

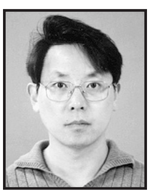
S. Ohbayashi, Renesas Technology, Itami, Japan

A wafer-level burn-in (WLBI) mode, a leak-bit redundancy and a small, highly reliable electrically trimmable (e-trim) fuse repair scheme for an embedded 6T-SRAM is used to achieve a known-good-die SoC. A 16Mb SRAM is fabricated with these techniques using a 65nm low-standby-power technology, and its operation is verified. The WLBI mode has a speed penalty of 50ps. The leak-bit redundancy area penalty is less than 2%.

27.3 A Continuous-Adaptive DDR2 Interface with Flexible Round-Trip-Time and Full Self Loop-Backed AC Test 2:30 PM

M. Haraguchi, Renesas Technology, Itami, Japan

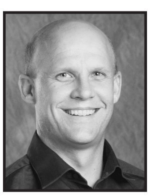
An experimental chip for a 32b wide DDR2 SDRAM interface for SoC is fabricated in a 90nm CMOS process and achieves 960Mb/s/pin operation. Impedance-calibration circuits and flexible round-trip circuits in a continuous-adaptive DDR2 interface are used to suppress skew and allow a longer round-trip time.



27.4 An 80nm 4Gb/s/pin 32b 512Mb GDDR4 Graphics DRAM with Low-Power and Low-Noise Data-Bus Inversion 3:15 PM

J-D. Ihm, Samsung Electronics, Hwasung, Korea

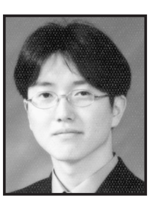
A 4Gb/s/pin 32b parallel 512Mb GDDR4 SDRAM is implemented in an 80nm DRAM process. It employs a data-bus inversion coding scheme with an analog majority voter insensitive to mismatch, which reduces peak-to-peak jitter by 21ps and voltage fluctuation by 68mV. A dual duty-cycle corrector is proposed to average duty error, and tuning is added to the auto-calibration of driver and termination impedance.



27.5 Phase-Tolerant Latency Control for a Combination 512Mb 2.0Gb/s/pin GDDR3 and 2.5Gb/s/pin GDDR4 SDRAM 3:45 PM

B. Johnson, Micron Technology, Boise, ID

A 512Mb graphics DRAM device uses phase-tolerant read and write latency control to achieve 2Gb/s/pin GDDR3 and 2.5G/ps/pin GDDR4 operation. The IC is implemented in a 95nm 1.5V triple metal CMOS process.



27.6 A DLL with Jitter-Reduction Techniques for DRAM Interfaces 4:15 PM

B-G. Kim, KAIST, Daejeon, Korea

A DLL featuring jitter-reduction techniques for a noisy environment is described. Loop behavior is controlled by monitoring the amount of jitter caused by supply noise of a replica delay line. The DLL is implemented in a 0.13μm CMOS process, and at 1GHz, it has $4.58ps_{rms}$ jitter and $29ps_{pp}$ jitter with noisy replica delay line.